Assessing AFEDC Architecture's Robustness to Timing Faults

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BACKGROUND & MOTIVATION

Fault Tolerant Solutions

- Limitations
  - Partial protection against soft errors
  - Sequential logic (SEU - Single Event Upsets) or combinational logic (SET - Single Event Transient)
  - Limited detection window
  - Unable to tolerate long pulse widths – 4.5ns
  - TMR is effective but not very efficient (area, power and time overheads)
  - High recovery penalties
  - Metastability problems

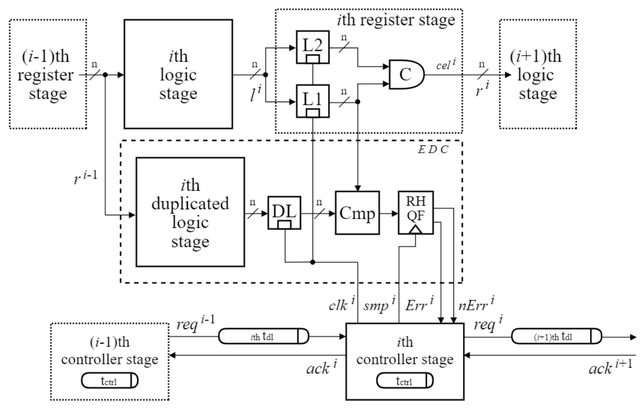
AFEDC Advantages

- Prevents metastability problems
- Tolerates SETs of unbounded duration
- Reduces error correction time penalties
- Reduces power and area when compared to TMR and synchronous counterparts
- Handles simultaneously SETs, SEUs, and **Timing Faults**

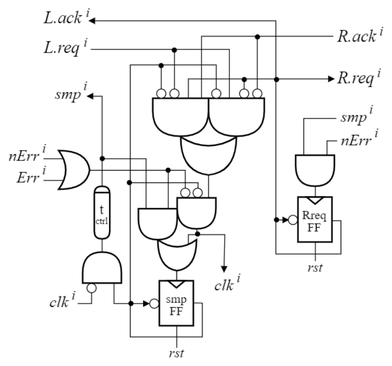
➔ **Timing faults robustness were not assessed until now**

Asynchronous Full Error Detection and Correction - AFEDC

- AFEDC soft error resilient architecture
  - Latch-based register
    - Dual Modular Redundant (DMR)
    - C-element as voter
- Bundled-data controller
  - 2-phase protocol
  - Click design
- Error Detection Circuit (EDC)
  - Full Duplication and Correction (FDC)
  - Q-Flop (QF) prevent metastability propagation

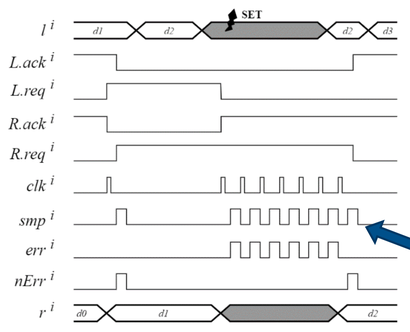


AFEDC architectures



AFEDC base Click controller

➔ **If an SET causes an error, the *Err* signal is flagged after the sample (*smp*). The controller then enters into a re-sampling loop (*clk->smp, clk->smp*…) where it stays until the error disappears**



AFEDC timing diagram

F. A. Kuentzer and M. Krstic, "Soft Error Detection and Correction Architecture for Asynchronous Bundled Data Designs," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 12, pp. 4883-4894, Dec. 2020.

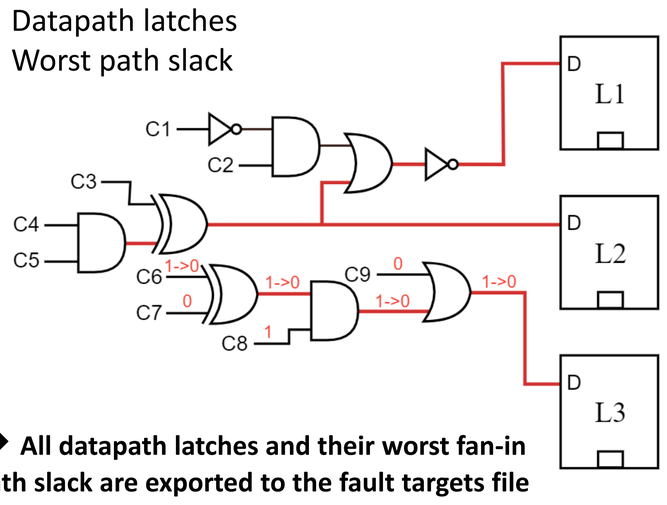
METHODOLOGY

Assessing AFEDC Robustness to Timing Faults

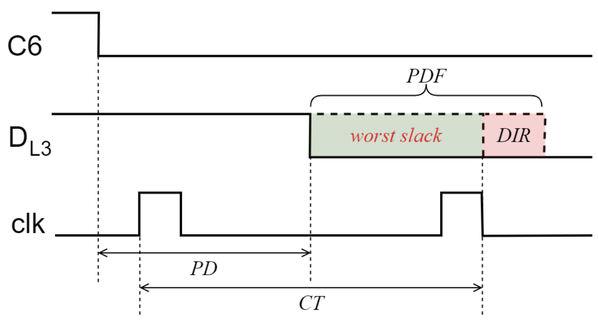
- AFEDC Custom Design Flow – Synopsys Design Compiler
  - Standard Delay Format (SDF)
  - AFEDC netlist

➔ **The fault targets are evaluated during the synthesis process**

- Fault target selection
  - Datapath latches
  - Worst path slack



➔ **All datapath latches and their worst fan-in path slack are exported to the fault targets file**



➔ **Adding the slack in the PDF turns each path into its worst case critical path, where even the smallest DIR has a high chance to generate a timing fault**

- Fault injection
  - Path Delay Fault (PDF)
  - Delay Increment Ratio (DIR)
  - Generate Mutant SDF

$$PDF_i = (CT \times DIR) + slack_i$$

- Golden Simulation
  - Number of Operations (NO)
  - maximum Cycle Time (CT)
  - Golden Simulation Time (GST)

➔ **Cadence Xcelium tools runs the testbench where for a defined NO, CT and GST are measured**

- Fault Simulation
  - Fault Simulation Time (FST)

➔ **For each fault simulation the FST and the throughput are measured for the defined NO**

- Fault classification
  - *On Time* **GST = FST**
  - *Delayed* **GST < FST**
  - *Premature* **GST > FST**

➔ **The fault classification is achieved by comparing all FSTs to the GST**

EXPERIMENTS AND OUTLOOK

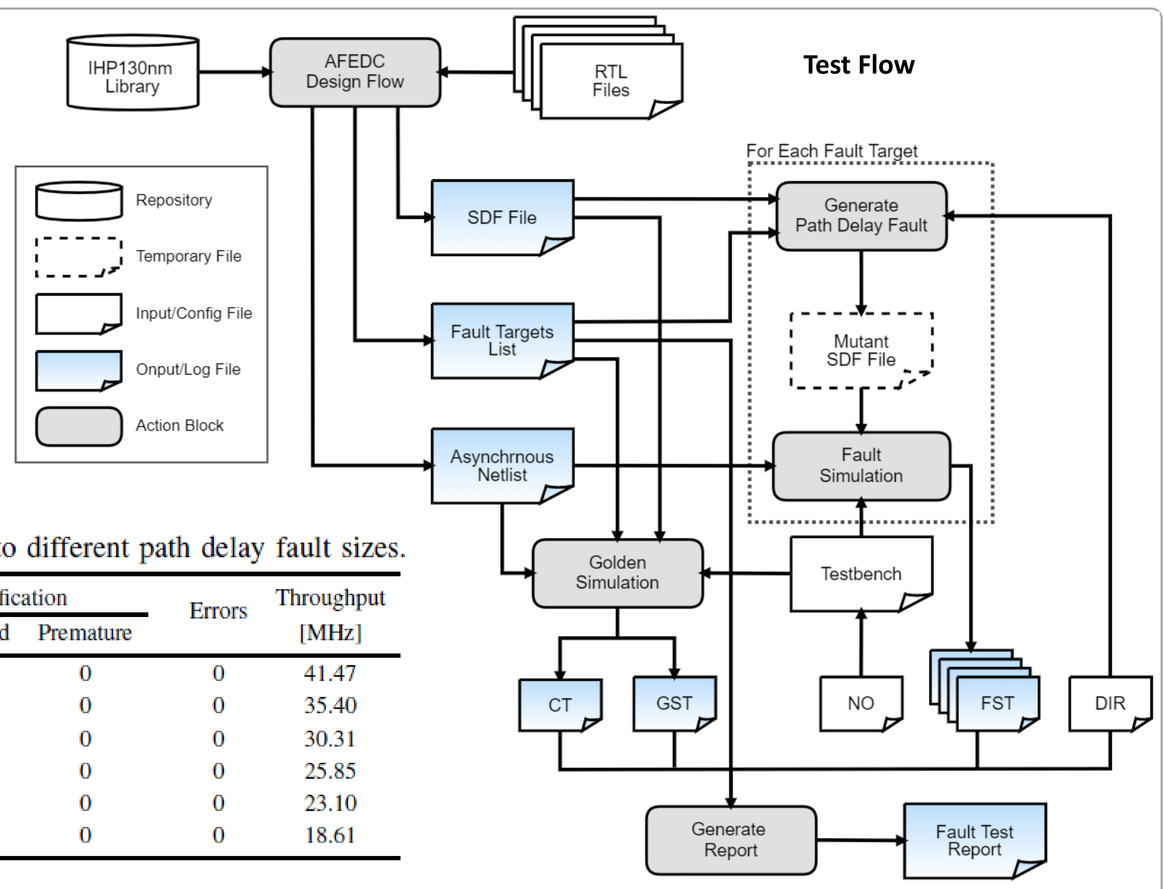
Timing Faults Evaluation

- Test case
  - AFEDC-FDC
  - 32-bit 5-stage pipeline non-restoring array divider
- IHP 130nm technology process
- Fault simulation parameters
  - **500** paths selected as **fault targets**
  - **CT** measured is 24.17ns (**41.47 MHz**)
  - **500** operations are computed by the array divider (**NO**)
  - Five different **DIR** experiments
    - **0.5, 1.0, 1.5, 2.0, 3.0**

➔ **Similar solutions will fail with 0.5 and above DIRs**

- Results
  - Not all fault simulations are *Delayed*
    - Paths with no transitions during simulation
    - Correct data latched despite the PDF injection
  - Errors are reported when the circuit does not produce the expected functional output
  - Performance lost is expected

➔ **Higher the DIR, lower the Throughput**



Test Flow

Golden Simulation

AFEDC fault tolerance to different path delay fault sizes.

DIR	Fault Classification			Errors	Throughput [MHz]
	On Time	Delayed	Premature		
-	500	0	0	0	41.47
0.5	72	428	0	0	35.40
1.0	4	496	0	0	30.31
1.5	4	496	0	0	25.85
2.0	4	496	0	0	23.10
3.0	4	496	0	0	18.61

➔ **The AFEDC can tolerate a wide range of timing faults and automatically adjust its cycle time while waiting for faulty paths to propagate correct data. These results open new ground for the AFEDC, where yield and aging properties can be explored**

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